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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,438	04/09/2004	Rong-Hui Kao	252011-2210	1354

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EXAMINER	
ULLAH, ELIAS	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,438	KAO ET AL.	
	Examiner	Art Unit	
	Elias Ullah	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *remarks filled on 8/8/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action remarks filled on 8/20/2006.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4,6,8,10, 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Tseng US 6,528,402.

1. As to claim 1 and 10. Tseng shows the method of forming an integrated circuit transistor, comprising: proving a semiconductor substrate (Fig. 2A, 40) with gate structure formed thereon (Fig. 2A, 44,46); forming at least one dielectric layer (42) overlying the semiconductor substrate, wherein the at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure (Fig. 2B) along the surface of the semiconductor substrate; forming at least one first doped region (48) in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one dielectric layer (42), wherein the at least one second portion of the at least one dielectric layer remains overlying the at least one first doped region (48, col. 3, lines 29-50) ; forming a sidewall spacer (50) overlying the at least one dielectric layer along the at least one sidewall of the gate structure; and forming at least one second doped region (52) in the semiconductor substrate laterally adjacent to the sidewall spacer.

2. As to claim 3, Tseng shows the method of forming integrated circuit transistor comprising a step of removing exposed regions of the at least one dielectric layer before formation of the at least one second doped region (col. 4, lines 23-58).

3. As to claim 2,4,12 and 13, Tseng shows the method of forming an integrated circuit transistor wherein a thickness of the at least one dielectric layer ranges from about 10 angstroms to about 350 Angstroms. The formation of the at least one dielectric layer is a blanket deposition of silicon oxide (col. 3, lines 42-44).

4. As to claim 6, 15, Tseng shows the method of forming an integrated circuit wherein the sidewall spacer is alternating layer of silicon oxide (col. 3, lines 54-55).

5. As to claim 8, Tseng shows the method of forming an integrated circuit transistor wherein the at least one first doped region is formed using an ion implantation process (col. 3, lines 45-47), and an annealing process (col. 4, lines 34-37).

3. As to claim 14, Tseng shows the shows the method of depositing at least one second dielectric layer overlying the at least one first dielectric layer, etching the at least one second dielectric layer to form at least one sidewall spacer along the at least one sidewall of the gate structure (col. 4, lines 53-58); and performing a second ion implantation process to form at least one second doped region in the semiconductor substrate laterally adjacent to the at least one sidewall spacer (52).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng in view of Samavedam et al. (6423632 dated 07/23/2002).

2. As to claim 5, Tseng shows the process as claimed and as described in the preceding paragraphs, but fails to expressly disclose the formation of the at least one dielectric layer is a blanket deposition by a chemical vapor deposition (CVD) process using tetraethylorthosilicate.

3. As to claim 5, Samavedam et al. teaches at least one dielectric layer (52) is a blanket deposition by chemical vapor deposition (CVD) process using tetraethylorthosilicate (TEOS) (col.4, lines 20-25). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dielectric layer as shown by Samavedam et al. because TEOS can be use to isolation of gate in the semiconductor transistors.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng in view of Perng et al. US 6,498,067.

5. As to claim 7, Tseng shows the process as claimed and as described in the preceding paragraphs, but fails to expressly disclose the sidewall spacer is formed using a blanket deposition process and a dry etch process.

6. As to claim 7, Perng et al. also teaches the method as claimed as: the sidewall spacer is formed using a blanket deposition process and a dry etch process (col. 4, lines 56-60, dry etch refer to RIE in the reference). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a sidewall as shown by Perng et al. because dry etch is used for an isotopic etch for sidewall.

6. Claim 9 and 11, are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng in view of Schuegraf et al. (6,140,203 dated 10/31/2000).

7. With respect to claim 9 and 11, Tseng shows the process as claimed and as described in the preceding paragraphs, but fails to expressly disclose the at least one dielectric layer becomes a densified material which exhibits an etch rate less than about 200 Angstroms/minute in a 100:1 HF solution.

With respect to claim 9 and 11, Schuegraf et al. teaches at least one dielectric layer (48) becomes a densified material, which exhibits rate less than about 200 Angstroms/minute in a 100:1 HF solution (48, col. 3, lines 40-45). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dense dielectric layer as shown by Schuegraf et al. in the claimed range because TEOS density can be also characterized relative to an etch rate of about 175 Angstroms/minute. Over lapping ranges establish a prima facie case of

obviousness. In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 514 F.2D 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Allowable Subject Matter

8. Claims 5,7,9 and are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following subject matter are allowable " CVD process using TEOS and forming sidewall spacer dry etch process."

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been fully considered but they are not persuasive. In response to applicant arguments " wherein the at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure, and at least one second portion outside the gate structure along the surface of the semiconductor substrate" that Tseng et al. fails to show. Tseng et al. teaches the at least one dielectric layer (Fig. 2A, 42) comprises at least one first portion along at least one sidewall of the gate structure (44, 46), and at least one second portion outside the gate structure along the surface of the semiconductor (Fig 2A, 42 overlaying outside of the substrate).

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Ullah whose telephone number is 571-272-1415. The examiner can normally be reached on 8-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MICHAEL LEBENTRITT can be reached on (571)272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E. Ullah

10/17/2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER